AICircuit: A Multi-Level Dataset and Benchmark for AI-Driven Analog Integrated Circuit Design

Asal Mehradfar[1] **Xuzhe Zhao**[2] **Yue Niu**[1] **Sara Babakniya**[1] **Mahdi Alesheikh**[2]
Hamidreza Aghasi[2] **Salman Avestimehr**[1]
[1] University of Southern California [2] University of California, Irvine

Abstract

Analog and radio-frequency circuit design requires extensive exploration of both circuit topology and parameters to meet specific design criteria. This design process is highly specialized and time-intensive, particularly as the number of circuit parameters increases and the circuit becomes more complex. Prior research has explored the potential of machine learning to enhance circuit design procedures; however, primarily focused on simple circuits. To date, a generic and diverse dataset with robust metrics on advanced mm-wave circuits does not exist. To bridge this gap, we present AICircuit, a comprehensive multi-level dataset and benchmark for developing and evaluating ML algorithms in analog and radio-frequency circuit design. AICircuit comprises seven commonly used advanced analog circuits and two complex wireless transceiver systems composed of multiple circuit blocks, encompassing a wide array of design scenarios encountered in real-world applications. We extensively evaluate various ML algorithms on the dataset, revealing the potential of ML algorithms in learning the mapping from the design specifications to the desired circuit parameters. The data and codebase are available in the following link: `https://github.com/AvestimehrResearchGroup/AICircuit`.

1 Introduction

By reaching the limits of Moore's Law [21] in early 2020, the exponential scaling of transistors, the core elements in circuit design, has become increasingly difficult, thereby slowing down the pace of advancements in semiconductor technologies. Unlike digital circuits, where scaling can often lead to straightforward performance improvements, analog and radio-frequency circuits should be custom-designed for emerging applications, e.g., mm-wave cellular communications, radar systems, and antenna systems, making their design both time-consuming and resource-intensive [17, 4, 9, 16, 1].

Conventional analog circuit design typically requires considerable effort and human involvement when searching the design space, including circuit topology and each circuit's parameters. Given a set of design specifications (e.g., power consumption, bandwidth, etc.), designers usually need first to decide the circuit topology and then conduct *circuit sizing* (i.e., parameter sweeping on each individual component), as shown in Figure 1. Among all the phases within the design of analog circuits, the complete schematic-level design is the most time-consuming part which may take up to a few weeks or months.

A few prior works investigate machine learning algorithms to automate analog circuit design [22, 11, 5, 15, 25, 6, 7]. In general, these methods train an ML model to learn the mapping between design specifications and actual circuit parameters. Despite progress in the prior works, current methods mainly show a proof of concept on simple circuits and systems such as two-stage voltage amplifiers. It still remains unclear how to scale current NN-based solutions on real-world analog systems with different components. In particular, a real-world system usually consists of different circuit blocks that perform different functions, such as a transmitter with an oscillator followed by a

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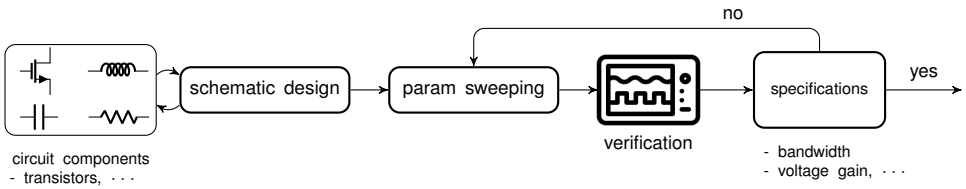

Figure 1: Conventional procedure of analog circuit design, which involves tremendous efforts to sweep in the parameter space to find the optimal design given design specifications.

power amplifier. Such systems introduce more complex mapping from inputs to outputs and exhibit high non-linearity. Furthermore, a high-quality dataset that includes various complex circuits is indispensable as a pivotal element in the ML-assisted circuit design.

In this work, we first introduce AICircuit, a multi-level circuit dataset and benchmark for training ML algorithms to assist various types of analog circuit design. In particular, the dataset consists of seven pivotal analog and radio-frequency circuits, i.e., common-source voltage amplifier (CSVA), cascode voltage amplifier (CVA), two-stage voltage amplifier (TSVA), low-noise amplifier (LNA), mixer, voltage-controlled oscillator (VCO), and power amplifier (PA). In addition, the dataset also consists of complex systems with multiple cascaded circuit components, which has not been investigated in prior works. AICircuit is a comprehensive collection of circuit parameters and simulated performance metrics from an accurate commercial simulator (Cadence Virtuoso). In addition to the dataset, we also conduct comprehensive evaluations on the benchmark dataset using various models ranging from conventional machine learning algorithms, such as random forest, to modern neural networks.

2 Problem Statement

In this work, we investigate the capabilities of machine learning algorithms in automating analog and radio-frequency circuit design. In particular, we evaluate machine learning algorithms on *homogeneous* and *heterogeneous* circuits. We define homogeneous circuits that compromise multiple circuits with identical functions. For instance, a two-stage voltage amplifier can be seen as a homogeneous circuit with two cascaded single-stage voltage amplifiers (Fig 10). On the other hand, we define heterogeneous circuits that compromise multiple circuit blocks with different functions, such as a transmitter with a voltage-controlled oscillator and a power amplifier (Fig 7a).

Machine Learning-Assisted Design. ML-assisted design usually adopts a reversed design flow compared to conventional circuit design. In particular, ML-assisted design takes a performance metric vector, $\boldsymbol{y}$, as inputs and uses a machine learning model $\mathcal{M}$ to predict a set of circuit parameters $\boldsymbol{x}$ as

$$\boldsymbol{x} = \mathcal{M}(\boldsymbol{y}), \tag{1}$$

The performance vector, $\boldsymbol{y}$, may contain DC power consumption, bandwidth, voltage gain, etc, which varies with circuit types. On the other hand, the circuit parameter vector, $\boldsymbol{x}$, describes the quantitative values of every component within the circuit, including resistances, capacitances, transistor widths, etc. Compared to conventional circuit design, ML-assisted methods directly learn the mapping from design specifications to circuit parameters, eliminating the need for parameter sweeping on $\boldsymbol{x}$ to find the solutions that meet the design specification in $\boldsymbol{y}$. Therefore, the whole design process can be significantly simplified.

As a key contribution in this work, we investigate the performance of different models on diverse circuits, ranging from a basic common-source amplifier to complex systems such as a transmitter with multiple heterogeneous circuit blocks.

3 Dataset

AICircuit consists of seven homogeneous and two heterogeneous circuits. For all circuits, we adopt the procedure as in Figure 2 to generate data. For a circuit, we first design a schematic using Cadence tools [14]. We defer details of circuit schematics in Appendix A. We then identify all key circuit parameters in the schematic that can affect the circuit performance. For each parameter, we set a value range, $[\texttt{beg}, \texttt{end}]$, and sweep the value with a small step size. For each parameter set, we run a

Cadence simulator to obtain the simulation results and calculate performance metrics. Each parameter set and the corresponding performance will be saved as one row in the dataset. After sweeping all parameters, we obtain a dataset with all possible design points. At last, we split the dataset into train and test sets for ML model training and testing.

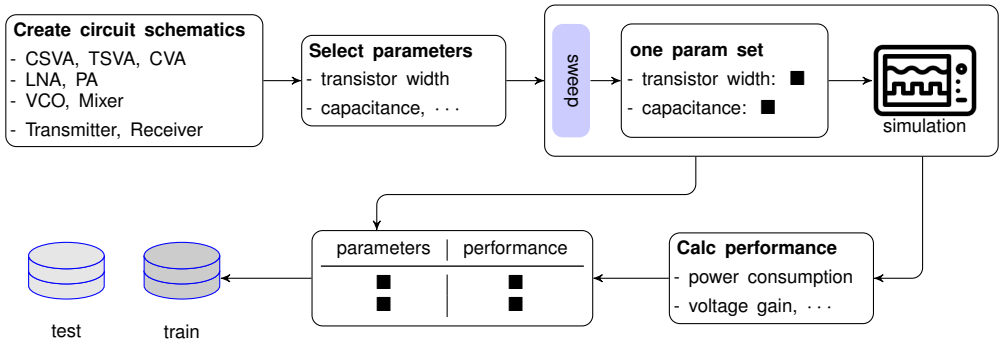

Figure 2: Procedure for creating datasets for commonly used analog circuits, including homogeneous and heterogeneous circuits.

3.1 Datasets for Homogeneous Circuit Blocks

We collect seven commonly used analog and radio-frequency circuits. Schematics of these circuits are provided in Appendix A. For each circuit, we select several circuit parameters that can greatly affect the design performance, as listed in Table 2. Based on the complexity of each circuit, a different number of parameters are considered in the simulation. The channel length of each transistor is fixed at 45 nm to simplify the design space and mitigate short-channel effects. These parameters are also the targets that an ML algorithm needs to predict given design specifications.

3.2 Datasets for Complex Heterogeneous Systems

In addition to basic homogeneous circuits, the work further investigates complex real-world millimeter-wave (mm-wave) circuit systems that contain multiple circuit blocks with different functions, as illustrated in Figure 7 [8]. In particular, we investigate a transmitter and a receiver operating at 28 GHz, which are commonly used in high-speed communication systems for sending and receiving mm-wave signals [13]. Table 1 lists design parameters to be optimized and the performance metrics to be examined. More details of these circuits are also provided in Appendix A.

Compared to basic homogeneous circuits, these heterogeneous circuits comprise a large parameter space to be optimized. Moreover, these systems exhibit increased non-linearity and intricate trade-offs between each block, leading to further challenges in learning the mapping from performance metrics to design parameters.

4 Evaluations

With the dataset collected from diverse circuits and complex radio-frequency systems, in this section, we train and evaluate multiple ML algorithms on the dataset and investigate their strengths and weaknesses.

Models. We test five different models: multi-layer perceptrons (MLPs), Transformers, support vector regressors (SVRs), random forest (RF), and K-nearest neighbors (KNNs). For all models, we feed the model with performance metrics and let the model predict the design parameters.

The transformer model [23] with the implementation based on [3] consists of one embedding layer, several encoder layers, and one fully connected layer for predicting a vector of circuit parameters. The multi-layer perception (MLP) model consists of seven fully connected layers, each intermediate layer having a rectified linear unit (ReLU) activation function. For support vector regressor (SVR), considering that SVR is a single-output regressor, we create multiple SVRs to predict all the circuit parameters. In particular, we fit one SVR per target parameter. To enhance non-linearity, we adopt

the `rbf` kernel [24] for each SVR model. In addition, RF regressors [2] combine the predictions from multiple decision trees and output the mean of their predictions to create a more accurate and stable prediction while KNNs locate the design parameters with performance close to input metrics. Details of each model are provided in Appendix B.

Metrics. In model training, we use ℓ_1 loss as the objective function that measures the distance between the predicted parameters and the desired parameters. In model evaluation, we further run a Cadence simulator given the predicted parameters and obtain the performance, $\hat{\boldsymbol{y}}$. We calculate the relative error compared to the desired performance specified in the dataset, $\boldsymbol{y}$. We report an individual error on each metric as

$$i\text{th metric} : err_i = \|\boldsymbol{y}_i - \hat{\boldsymbol{y}}_i\|/\boldsymbol{y}_i \tag{2}$$

End-to-End Training and Evaluation. Our codebase provides an end-to-end model training and evaluation pipeline, as shown in Figure 3. It enables a smooth interaction between the ML workflow and the analog circuit workflow. During the training stage, we simply follow the standard ML workflow to load data and train the model. During the evaluation phase, we first obtain the predicted parameters via the ML workflow and then call the Cadence simulator to compute the actual performance and the relative error compared to the desired value. Importantly, by including a Cadence simulator in the evaluation pipeline, we can accurately obtain metrics with inherent randomness based on advanced analyses, such as the noise figure in a low-noise amplifier and the phase noise in a voltage-controlled oscillator, which were not seen in prior works. More details are provided in Table 2 and 1.

train

```
def Train(model, trainset):
  for _ in range(maxIter):
    x, y = loadData(trainset)
    xPred = model(y)
    loss = calcLoss(x, xPred)
    # update model
    model.fit(x, y)
```

evaluation

```
def Eval(model, evalset, simulator):
  for _ in range(maxIter):
    x, y = loadData(evalset)
    xPred = model(y)
    # circuit workflow
    # simulator: simulator class with
       all circuit information
    yPred = simulator.run(xPred)
    error = calcError(y, yPred)
```

simulation

```
class Simulator():
  ...
  ...
  def run(self, xPred):
    alterCircParam(xPred)
    # call Cadence simulator
    call(cadenceCommand)
    yPred = parseResults()
```

Figure 3: An end-to-end model training and evaluation pipeline.

4.1 Homogeneous Circuit Blocks

We first evaluate ML algorithms on homogeneous circuits. In particular, we show the results of MLP, Transformer, SVR, and RF on a two-stage voltage amplifier (TSVA) in the main paper (Figure 4) and defer other results of other circuits in Appendix D. To better present the results, we plot the distribution of relative errors (See Eq(2)) of all metrics.

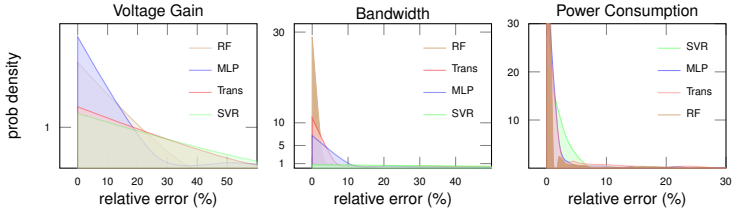

Figure 4: Two-Stage Voltage Amplifier

Summary. Across all circuits in this section, we observe that ML models perform well in learning the relationship between circuit parameters and simple performance metrics such as the DC power consumption. Importantly, the observation holds regardless of the complexity of the circuits. The reason is that the simple performance metrics usually exhibit a linear relation with circuit parameters, which makes it easy to predict. However, as the relationship becomes more non-linear, learning the relationships tends to be more challenging, even for MLPs and Transformers. For instance, voltage gain in a two-stage voltage amplifier, conversion gain in a mixer, phase noise in VCO, and performance metrics in PA are highly non-linear in relation to the circuit parameters. As a result, these circuits predicted by ML models do not result in performance very close to the desired specifications.

4.2 Heterogeneous Radio-Frequency Systems

Moving from homogeneous circuits to heterogeneous ones, the number of performance metrics and circuit parameters increases. Furthermore, as heterogeneous circuits comprise multiple circuits, the relationship between circuit parameters and performance is further complicated. Therefore, evaluations on heterogeneous circuits provide more insights into how ML algorithms learn to predict complex circuits. More results are provided in Appendix D.

Transmitter. In a transmitter system comprising VCO and PA, we can observe in Figure 5 that as the circuit becomes more complex, circuit parameters are harder to predict to meet the desired specification. Models such as SVR and RF lack sufficient capacity to predict complex systems, resulting in large errors. MLPs and transformers, on the other hand, predict circuits with much smaller errors. However, they still struggle to give a design that meets certain complex specifications, such as output power.

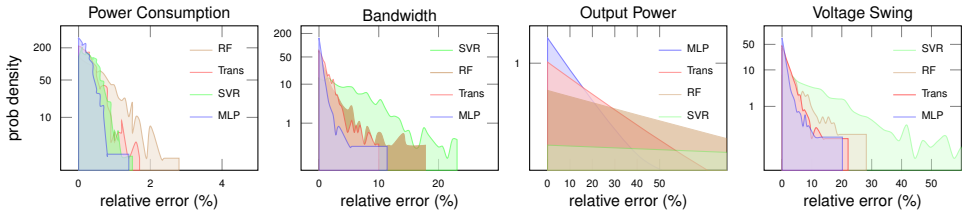

Figure 5: Transmitter (VCO and PA) system-level metrics.

Receiver. We further evaluate ML models on a receiver system comprising an LNA, a mixer, and a CVA. Compared to the transmitter system, circuits in the receiver are less complex. Therefore, models such as MLPs and transformers can predict circuits with smaller errors compared to the desired specifications (Figure 6). Besides, since the training dataset of the receiver includes more circuit parameters than the transmitter, the trained models exhibit better generalization performance with more training data points.

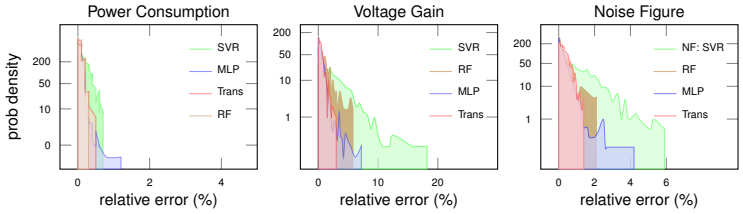

Figure 6: Receiver (LNA, Mixer, and CVA)

Summary. Throughout the evaluations of a transmitter and a receiver system, we can observe how the performance of ML algorithms is affected by the complexity of circuits. From a receiver to a transmitter, the relationship between circuit parameters and the performance becomes more non-linear. As a result, it is more challenging to predict a circuit that meets design specifications.

5 Conclusion

In this work, we propose a multi-level benchmark dataset for analog and radio-frequency circuit design. The proposed dataset, AICircuit, covers homogeneous and heterogeneous circuits. Homogeneous circuits comprise one or multiple circuits with identical functions, while heterogeneous circuits comprise circuits with different functions. We evaluate various machine learning algorithms on the benchmark datasets, including multi-layer perceptrons (MLPs), transformers, and support vector regression (SVRs). The evaluations provide a comprehensive overview of the strengths and weaknesses of each method. In a word, MLPs and Transformers usually give better designs compared to other methods, especially for complex circuits. We also reveal that for complex circuits, further optimization of model design and training are still needed to improve the design.

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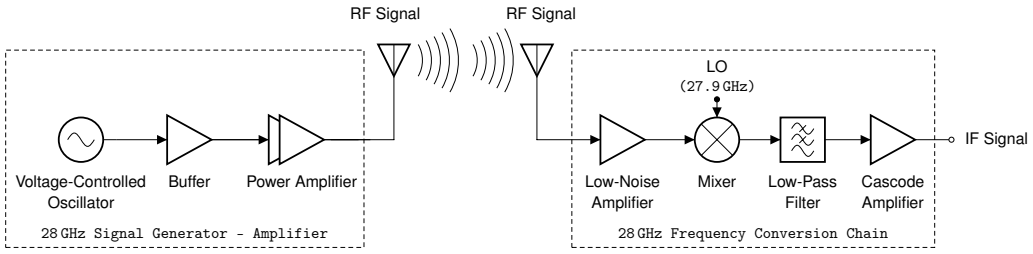
A Circuits

Homogeneous Circuits. Among the homogeneous circuits, the analog voltage amplifiers, including the common-source voltage amplifier (CSVA), cascode voltage amplifier (CVA), and two-stage voltage amplifier (TSVA), are essential for voltage amplification, a critical function in most analog circuits and feedback systems [20]. CSVA is a versatile and widely used component in analog and radio-frequency circuit design. It receives input at the *gate* terminal and generates amplified output at the *drain* terminal (See Figure 8). By combining the *common-source* (CS) and *common-gate* (CG) stages, CVA can provide enhanced gain and improved bandwidth over CSVA, which is suitable for high-frequency applications (Figure 9). TSVA further improves the output swings in the cascode configuration and obtains high gains (Figure 10).

In addition to voltage amplifiers, the dataset also covers other types of circuits in radio-frequency applications, including the low-noise amplifier (LNA), mixer, voltage-controlled oscillator (VCO), and power amplifier (PA). In particular, the cascode LNA in a radio-frequency receiver front-end provides substantial power gain while maintaining low noise across a wide bandwidth range (Figure 11). An active mixer is used for frequency modulation with conversion gain in radio-frequency transmitters and receivers. VCO generates a periodic signal with frequency tuned across a wide range controlled by a voltage signal. Owing to the low phase noise and power consumption, the cross-coupled VCO has become a prevalent configuration to provide sustainable oscillation (Figure 13). The two-stage differential PA, the most power-intensive building block in the radio-frequency transmitter, plays a crucial role in delivering significant power to the transmitting antenna without compromising efficiency (Figure 14).

Heterogeneous Circuits. For a transmitter, we combine the voltage-controlled oscillator (VCO) and power amplifier (PA) as a typical *signal generator – amplifier* system (Figure 7a) [19]. The system first generates a periodic signal via a VCO with tunable frequency and then amplifies the signal by the PA with substantial power gain. For a receiver, we establish a classical *frequency conversion* chain by integrating the low-noise amplifier (LNA) with a mixer and cascode voltage amplifier (CVA) (Figure 7b) [12]. With a signal received from an antenna, an LNA is first applied to amplify the weak input signal without introducing undesired noise. Then, a mixer is involved in converting the signal from radio frequency to intermediate frequency (IF) [18]. The output IF signal is then amplified by a CVA that serves as an IF amplifier for further processing. There are two additional blocks, buffer and low-pass filter, shown in the transmitter and receiver. As their topology and parameters are usually fixed, we do not optimize them in the pipeline.



(a) Transmitter system (b) Receiver system

Figure 7: 28 GHz wireless transceiver circuits. (a) Transmitter architecture involving VCO and PA. Buffer used here to sustain system stability; (b) Receiver architecture comprising LNA, Mixer, and CVA. Low-Pass Filter deployed here to filter out the undesired high frequency components.

Schematics and Design Trade-offs. In this section, we provide details on the examined homogeneous and heterogeneous circuits in Section 3 and 4. As mentioned in the body of the paper, time-consuming parametric sweeps are necessary for designing analog and radio frequency circuits. Often, a small subset of design parameters can satisfy the thresholds for design metrics. From a circuit design perspective, the limited number of parameter combinations that satisfy the metrics happens due to: 1) the complexity of transistor models and the sensitivity of their operation to surrounding circuit elements, circuit configuration, bias conditions, size of the transistor, etc. 2) inherent trade-offs among various design metrics in each circuit. In what follows, for each circuit, in addition to the schematics and set of design parameters and metrics, multiple important design trade-offs are listed

within colored boxes adjacent to the schematics. The same color is reserved for a trade-off if it is present in more than one circuit.

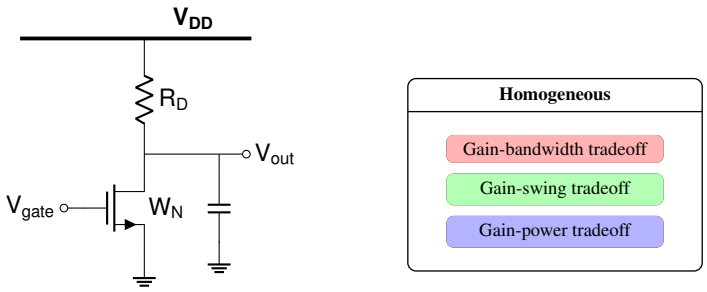


Figure 8: Common-Source Voltage Amplifier.

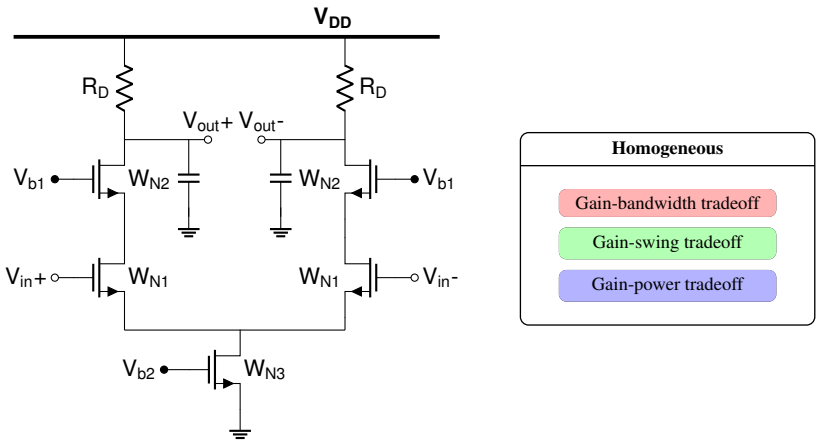


Figure 9: Cascode Voltage Amplifier.

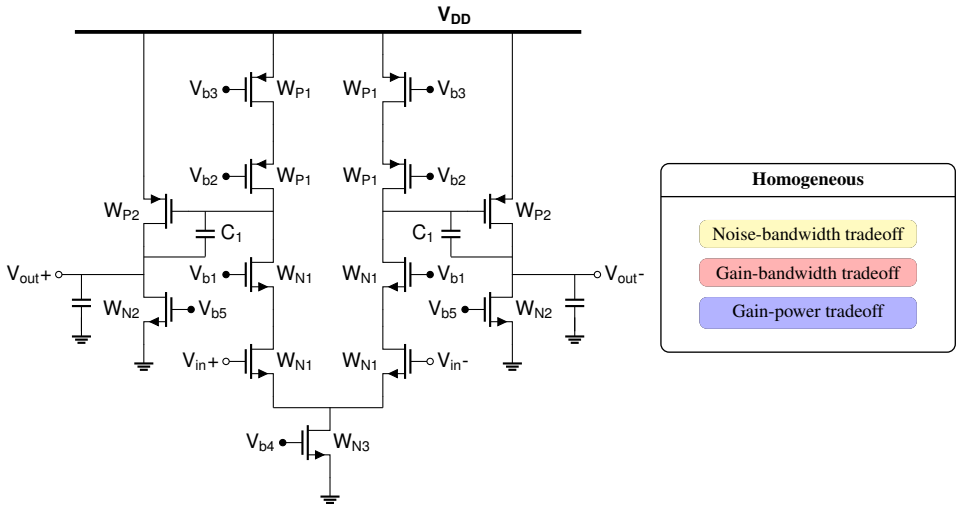


Figure 10: Two-Stage Voltage Amplifier.

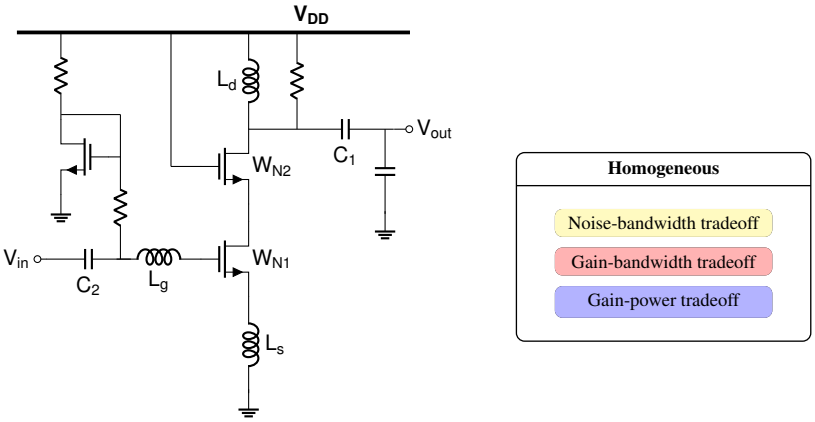


Figure 11: Low-Noise Amplifier.

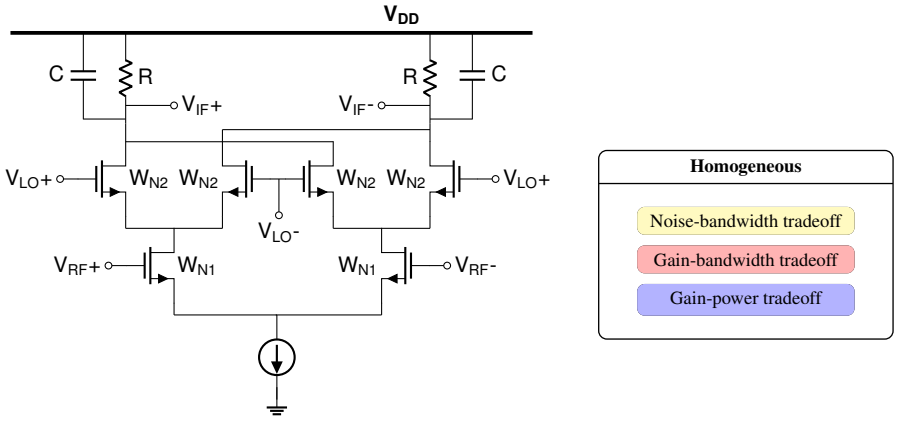


Figure 12: Mixer.

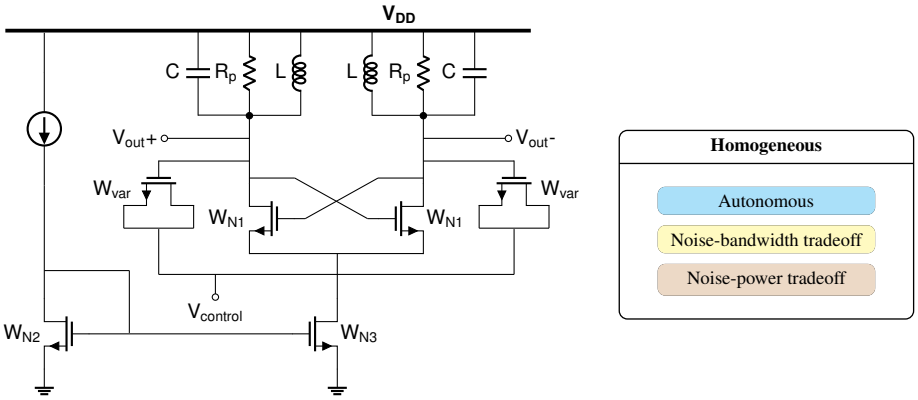


Figure 13: Voltage-Controlled Oscillator.

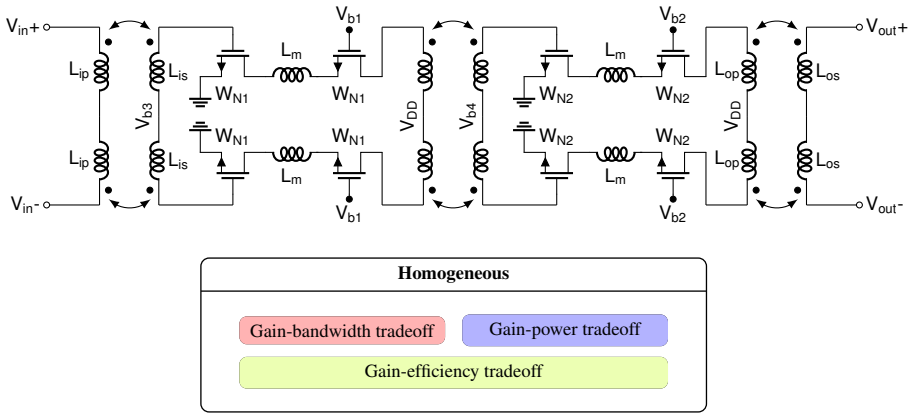


Figure 14: Power Amplifier.

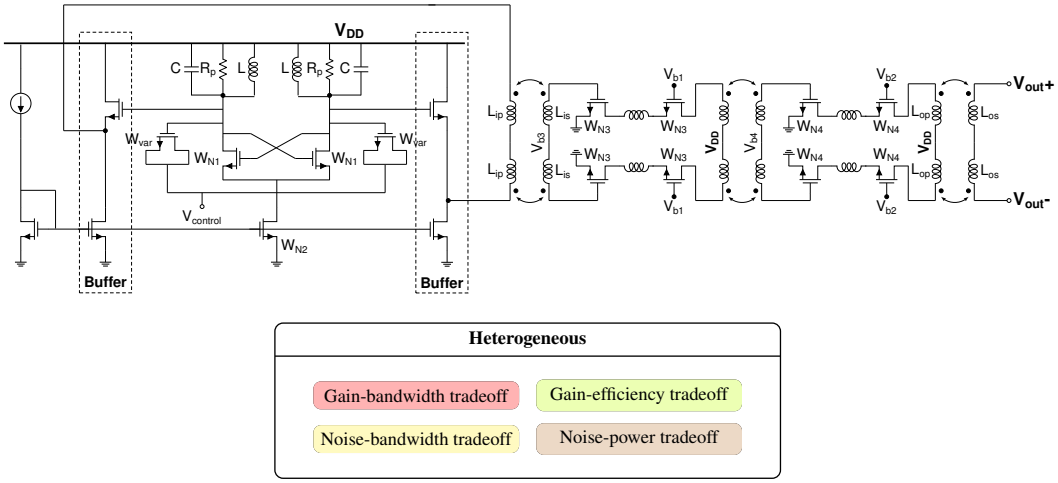


Figure 15: Heterogeneous system on the transmitter side.

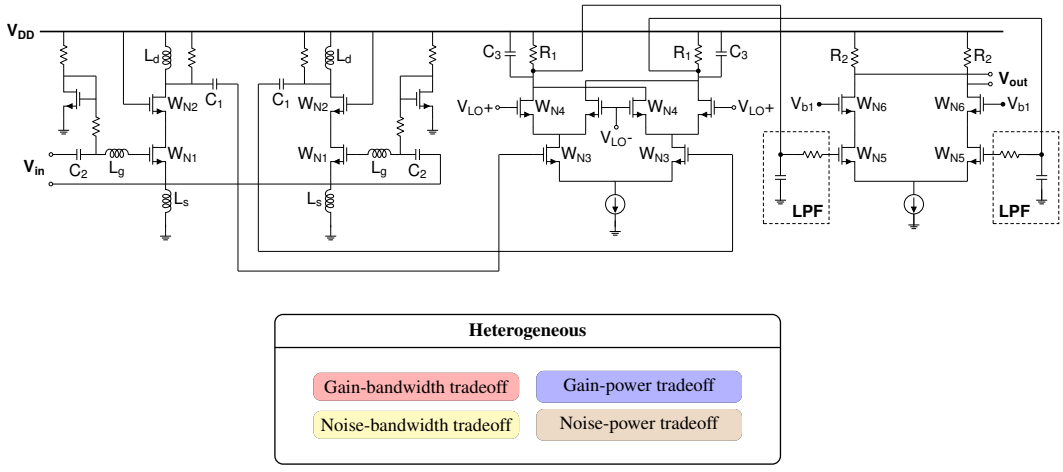


Figure 16: Heterogeneous system on the receiver side.

Heterogeneous Circuits	**Individual Block**	**Parameter**	**Sweeping Range**
Transmitter System **specs**: dc power | bandwidth | output power | voltage swing	Voltage-Controlled Oscillator (VCO) **specs**: phase noise | tuning range	C	50:50:150 (fF)
		L	60:60:180 (pH)
		R_p	300:100:500 (Ω)
		W_{N1}	7.5:2.5:12.5 (μm)
		W_{N2}	187.5:12.5:212.5 (μm)
		W_{var}	70:10:90 (μm)
	Power Amplifier (PA) **specs**: power gain | drain efficiency | PAE	L_{ip}	175:175:350 (pH)
		L_{is}	60:60:120 (pH)
		L_{op}	360:353:713 (pH)
		L_{os}	45:45:90 (pH)
		W_{N3}	22:5:32 (μm)
		W_{N4}	16:5:26 (μm)
Receiver System **specs**: dc power | gain | noise figure	Low-Noise Amplifier (LNA) **specs**: power gain | S_{11} | noise figure	C_1	130:50:180 (fF)
		C_2	170:50:220 (fF)
		L_d	180:50:230 (pH)
		L_g	850:100:950 (pH)
		L_s	80:10:90 (pH)
		W_{N1}	20:3:26 (μm)
		W_{N2}	37.5:2.5:42.5 (μm)
	Mixer **specs**: voltage swing | conversion gain	C_3	1:0.1:1.1 (pF)
		R_1	400:100:500 (Ω)
		W_{N3}	14:2:18 (μm)
		W_{N4}	6:2:10 (μm)
	Cascode Voltage Amplifier (CVA) **specs**: gain	R_2	300:100:400 (Ω)
		W_{N5}	26:2:30 (μm)
		W_{N6}	14:2:18 (μm)

Table 1: Heterogeneous circuits and the chosen parameters for each block. The sweeping range of selected design parameters is written in the form of [`beg`, `increment`, `end`]. Detailed circuit topology is provided in Appendix A. Specs of each circuit are explained in Appendix C.

Homogeneous Circuit	Parameter	Description	Sweeping Range
Common-Source Voltage Amplifier (CSVA) **specs**: dc power | bandwidth | gain	V_{DD}	supply voltage	1.2:0.1:1.8 (V)
	V_{gate}	gate voltage	0.6:0.05:0.9 (V)
	R_D	load resistor	0.5:0.1:3 (kΩ)
	W_N	width of nmos	3:1:10 (μm)
Cascode Voltage Amplifier (CVA) **specs**: dc power | bandwidth | gain	R_D	load resistor	0.5:0.1:2 (kΩ)
	W_{N1}	width of nmos	6:1:17 (μm)
	W_{N2}	width of nmos	5:1:12 (μm)
	W_{N3}	width of nmos	4.5:0.5:9 (μm)
Two-Stage Voltage Amplifier (TSVA) **specs**: dc power | bandwidth | gain	C_1	miller capacitor	150:50:250 (fF)
	W_{P1}	width of pmos	10:1:18 (μm)
	W_{P2}	width of pmos	7.5:5:22.5 (μm)
	W_{N1}	width of nmos	10:1:18 (μm)
	W_{N2}	width of nmos	7.5:5:22.5 (μm)
	W_{N3}	width of nmos	16:2:24 (μm)
Low-Noise Amplifier (LNA) **specs**: dc power | bandwidth | power gain | S_{11} | noise figure	C_1	output capacitor	300:100:600 (fF)
	C_2	input capacitor	200:100:500 (fF)
	L_d	drain inductor	3:1:5 (nH)
	L_g	gate inductor	8.4:1:11.4 (nH)
	L_s	source inductor	0.6:0.1:0.8 (nH)
	W_{N1}	width of nmos	25:1.25:30 (μm)
	W_{N2}	width of nmos	25:1.25:30 (μm)
Mixer **specs**: dc power | voltage swing | conversion gain | noise figure	C	coupling capacitor	0.5:0.1:1.5 (pF)
	R	load resistor	200:25:500 (Ω)
	W_{N1}	width of nmos	15:1:25 (μm)
	W_{N2}	width of nmos	5:1:15 (μm)
Voltage-Controlled Oscillator (VCO) **specs**: dc power | frequency | phase noise | tuning range	C	capacitor in resonant tank	100:25:200 (fF)
	L	inductor in resonant tank	2:1:6 (nH)
	R_p	parallel resistor	1:1:4 (kΩ)
	W_{N1}	width of nmos	24:8:56 (μm)
	W_{N2}	width of nmos	11:1:12 (μm)
	W_{N3}	width of nmos	96:32:160 (μm)
	W_{var}	width of nmos capacitor	75:12.5:125 (μm)
Power Amplifier (PA) **specs**: dc power | S_{11} | S_{22} | power gain | PAE | drain efficiency | P_{sat}	L_{ip}	input primary inductor	175:175:525 (pH)
	L_{is}	input secondary inductor	40:40:120 (pH)
	L_m	inter-stage matching inductor	87.5:87.5:263 (pH)
	L_{op}	output primary inductor	238:238:714 (pH)
	L_{os}	output secondary inductor	30:30:90 (pH)
	W_{N1}	width of nmos	16:3:28 (μm)
	W_{N2}	width of nmos	24:4:40 (μm)

Table 2: Homogeneous circuits and the chosen parameters for each circuit. The sweeping range of selected design parameters is written in the form of $[\texttt{beg}, \texttt{increment}, \texttt{end}]$. Detailed circuit topology is provided in Appendix A. Specifications of each circuit are explained in Appendix C.

B Implementation Details

As the performance metrics and parameters targeted by the models have different ranges, we first apply the preprocessing and normalize the data to $[-1, 1]$. For training data splitting, we randomly sample 90 percent of the data points as the training dataset, and 10 percent as the test dataset. We train the neural networks (transformer and MLP) for 100 epochs using the Adam optimizer [10] with a learning rate of 0.001. Each training is conducted several times to ensure that our methods are robust to random seeds.

Model	Parameter	Description	Value
Transformer	`dim_model`	first fully connected layer dim	200
	`num_heads`	heads in the multi-head attention models	2
	`dim_hidden`	load resistor	200
	`dropout_p`	the dropout probability	0.1
	`num_encoder_layers`	number of layers in transformer encoder	6
	`activation`	activation function of transformer encoder	relu
Multi Layer Perception (MLP)	`num_layers`	number of fully connected layers	7
	`dim_layers`	dimension of layers	[200, 300, 500, 500, 300, 200]
Support Vector Regressor (SVR)	`kernel`	kernel type of the algorithm	rbf
	`multi_target_regression_type`	type of combining multiple SVRs	MultiOutputRegression
K Nearest Neighbors Regressor (KNN)	`n_neighbors`	number of neighbors	5
	`weights`	weight function used in prediction	uniform
Random Forest Regressor (RF)	`n_estimators`	number of trees in the forest	100
	`criterion`	function to measure the quality of a split	squared_error (l_2 Loss)

Table 3: Models and the chosen parameters for each model.

Circuit	CSVA	CVA	TSVA	LNA	Mixer	VCO	PA	Transmitter	Receiver
Dataset Size	7.8k	15.1k	19.3k	32k	17.1k	13.5k	5.6k	95.3k	155.4k

Table 4: Number of data points for each circuit.

C Specifications of Each Circuit

In this section, we review the definitions of various performance metrics that are simulated for the homogeneous and heterogeneous circuits in this work.
Voltage gain of an amplifier, denoted commonly as A_v, is the ratio of the output amplified voltage V_{out} to the input voltage V_{in} in an amplifier circuit.

$$A_v = \frac{V_{out}}{V_{in}} \tag{3}$$

Bandwidth is the range of frequencies over which an amplifier can operate effectively, defined by the difference between the upper and lower cutoff frequencies.

$$BW = f_{high} - f_{low} \tag{4}$$

For amplifiers with low-pass profile, the bandwidth is defined as the frequency at which the dB amount of voltage gain drops from the low-frequency gain by 3 dB.
The total power that the circuit draws from the power supply is known as **power consumption**, and it is calculated as the product of supply voltage and supply current.

$$P = V_{supply} \times I_{supply} \tag{5}$$

Conversion gain is the measure of the signal amplification in a mixer, expressed in decibels, comparing the output signal to the input signal.

$$CG = 20 \log \left(\frac{V_{out}}{V_{in}} \right) \text{ dB} \tag{6}$$

Noise figure is the ratio of the input signal-to-noise ratio to the output signal-to-noise ratio, expressed in decibels, indicating the noise performance of a low-noise amplifier, mixer, or receiver chain.

$$NF = 10 \log \left(\frac{SNR_{in}}{SNR_{out}} \right) \text{ dB} \tag{7}$$

Intermediate frequency (IF) **voltage swing** refers to the peak-to-peak voltage of the mixer's intermediate frequency signal.

The **oscillation frequency** is the frequency at which the oscillator produces its periodic signal, which is normally controlled by the circuit's inductance and capacitance in an LC-based oscillator.

$$f_{\text{osc}} = \frac{1}{2\pi\sqrt{LC}} \tag{8}$$

The power that the oscillator provides to a given load is known as **output power**, and it is computed by dividing the root-mean-square (RMS) output voltage squared by the load resistance.

$$P_{\text{out}} = \frac{V_{\text{out,RMS}}^2}{R_{\text{load}}} \tag{9}$$

Phase noise is a measure of the oscillator's frequency stability, representing the noise power in a 1 Hz bandwidth at a specific offset frequency from the carrier, relative to the carrier power, where $S_\phi(f)$ is the phase noise power spectral density.

$$L(f) = 10 \log \left(\frac{S_\phi(f)}{2P_{\text{carrier}}} \right) \text{ dBc/Hz} \tag{10}$$

The oscillator's **tuning range** is the range of frequencies that it can be adjusted over, measured from maximum to minimum.

$$TR = f_{\text{max}} - f_{\text{min}} \tag{11}$$

S_{11} represents the ratio of the reflected voltage wave to the incident voltage wave at the power amplifier's input, which shows how much of the input signal is reflected.

$$S_{11} = \frac{V_{reflected,1}}{V_{incident,1}} \tag{12}$$

S_{22} represents the ratio of the reflected voltage wave to the incident voltage wave at the power amplifier's output, which shows how much of the output signal is reflected.

$$S_{22} = \frac{V_{reflected,2}}{V_{incident,2}} \tag{13}$$

Large signal gain is the ratio of the output power to the input power of the amplifier under large signal conditions.

$$G_{\text{LS}} = 20 \log \left(\frac{P_{out}}{P_{in}} \right) \text{ dB} \tag{14}$$

Power added efficiency is the amplifier's efficiency in converting DC power into radio frequency output power while taking input power into account.

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \times 100\% \tag{15}$$

Drain efficiency is defined as the ratio of radio frequency output power to total DC power consumed by the amplifier.

$$DE = \frac{P_{out}}{P_{DC}} \times 100\% \tag{16}$$

Saturated power or Psat denotes the highest possible output power level that a power amplifier can produce upon reaching saturation. Up until this point, increasing the input power further does not significantly increase the output power.

$$P_{\text{sat}}(\text{dBm}) = 10 \log_{10} \left(\frac{P_{\text{sat}}(\text{mW})}{1\text{mW}} \right) \tag{17}$$

Power gain is a measure of how much a circuit increases the power of a signal from its input to its output.

$$G_P = \frac{P_{\text{out}}}{P_{\text{in}}} \tag{18}$$

Voltage-controlled oscillator's (VCO) output power is the amount of electrical power delivered at its output terminal. The output power P_{out} is proportional to the square of the RMS voltage V_{rms} and the load resistance R_{load}.

$$P_{\text{out}} = \frac{1}{2} \cdot V_{\text{rms}}^2 \cdot R_{\text{load}} \tag{19}$$

Transmitter output power is the amount of electrical power delivered by the transmitter to the antenna for transmission as electromagnetic waves.

$$P_{\text{out}} = P_{\text{in}} \cdot G_t \tag{20}$$

where, P_{out} is the transmitter output power. P_{in} is the input power to the transmitter, and G_t is the gain of the transmitter.

Transducer Gain (G_t **)** of Low Noise Amplifier (LNA) refers to the ratio of the output signal power to the available input signal power which includes the matching effect as well.

$$G_T = \frac{P_{\text{out}}}{P_{\text{in}}} \tag{21}$$

D Results on More Circuits

Results on Mixer.

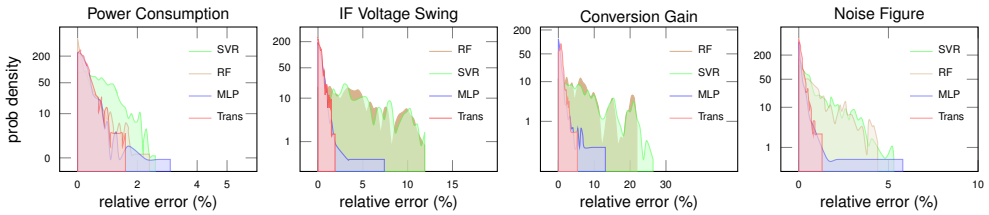


Figure 17: Mixer

Results on Voltage-Controlled Oscillator (VCO).

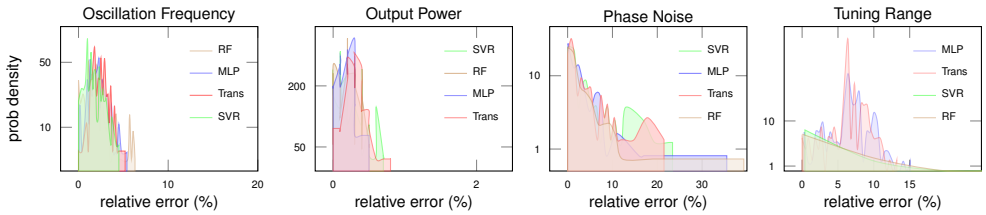


Figure 18: Voltage-Controlled Oscillator

Results on Power Amplifier (PA).

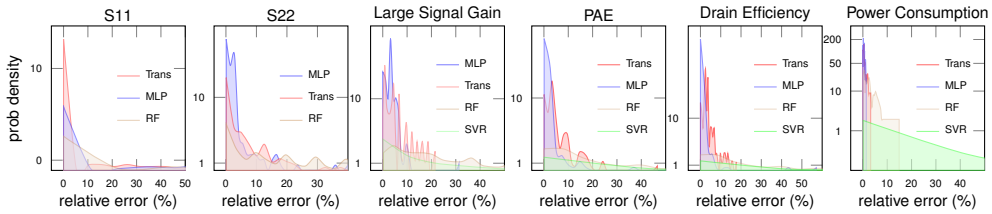


Figure 19: Power Amplifier

Results on Common-Source Voltage Amplifier (CSVA).

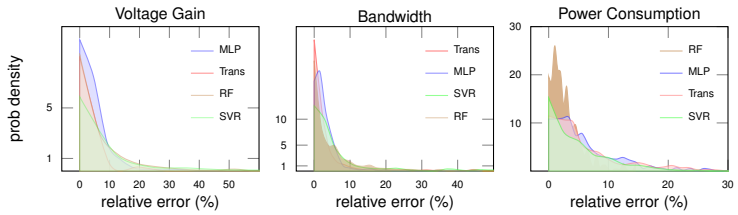


Figure 20: Common-Source Voltage Amplifier

Results on Cascode Voltage Amplifier (CVA).

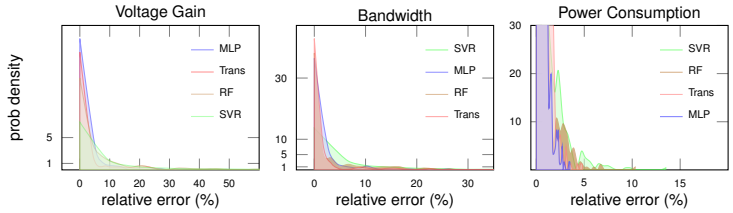


Figure 21: Cascode Voltage Amplifier

Results on Low-Noise Amplifier (LNA).

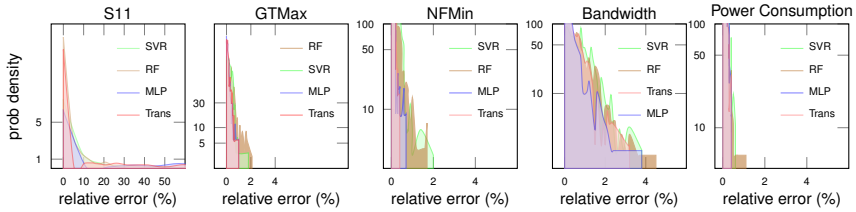


Figure 22: Low-Noise Amplifier

Results on Transmitter.

For the metrics of individual components, circuits predicted by MLPs and transformers still result in smaller errors compared to SVRs and RF. One interesting observation is that, as more performance metrics are involved in learning a heterogeneous circuit, the trained models can generate circuits with small errors on individual metrics (e.g., the tuning range of VCO compared to Fig 18).

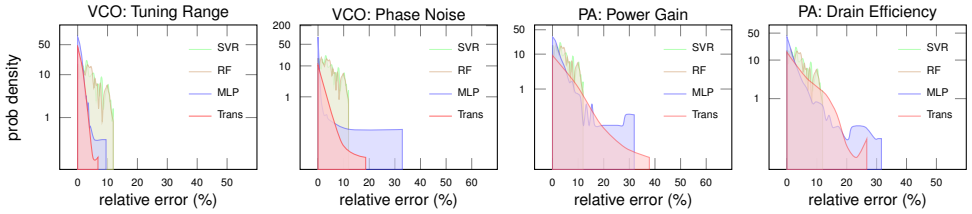


Figure 23: Transmitter (VCO and PA) metrics for individual components.

Results on KNN.

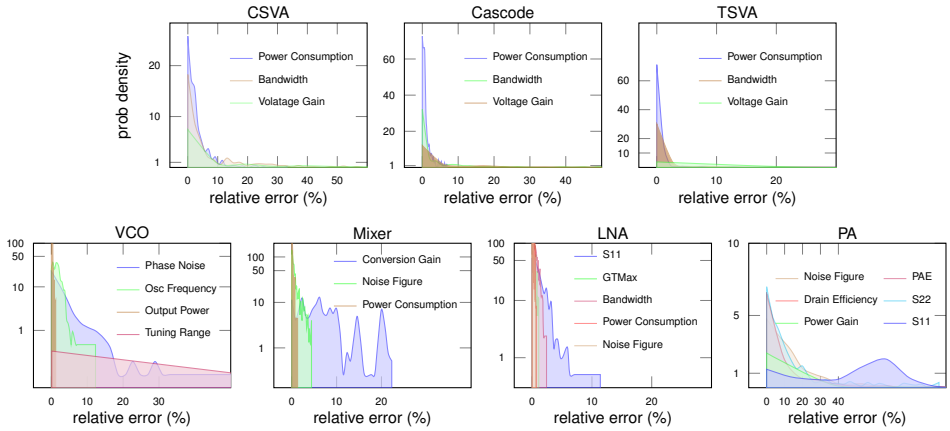


Figure 24: KNN performance on homogeneous circuits.